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1 Mechanism and device-to-device variation of leakage current in polysilicon thin film transistors

Wu, I.-W.; Lewis, A.G.; Huang, T.-Y.; Jackson, W.B.; Chiang, A.;
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Pages:867 - 870

[\[Abstract\]](#) [\[PDF Full-Text \(272 KB\)\]](#) IEEE CNF

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Amarh, F.; Karady, G.G.; Sundararajan, R.;
Power Delivery, IEEE Transactions on, Volume: 17, Issue: 4, Oct. 2002
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4 Reverse leakage current calculations for SiC Schottky contacts

Crofton, J.; Sriram, S.;
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5 Improved wafer-level spatial analysis for I_{DDQ} limit setting

Sabade, S.; Walker, D.M.H.;
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Pages:82 - 91

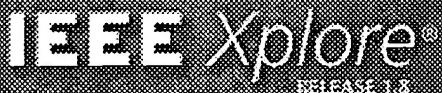
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6 On the calculation of the quasi-bound-state energies and lifetimes in inverted MOS structures with ultrathin oxides and its application to the direct tunneling current

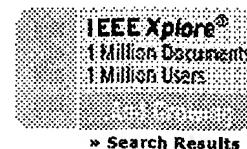
Govoreanu, B.; Magnus, W.; Schoenmaker, W.; Van Houdt, J.; De Meyer, K.;
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[\[Abstract\]](#) [\[PDF Full-Text \(416 KB\)\]](#) IEEE JNL

7 Influence of substrate current on hold-time characteristics of dynamic MOS IC's



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1 Built-in self test for C-testable ILA's

Gala, M.; Ross, D.; Watson, K.; Vasudevan, B.; Utama, P.;
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Yih, J.-S.; Mazumder, P.;
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Pages:62 - 66

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5 Performance of signature registers in the presence of correlated errors

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Pages:393 - 400

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6 Enhanced DO-RE-ME based defect level prediction using defect site aggregation-MPG-D

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